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US 4144414 A

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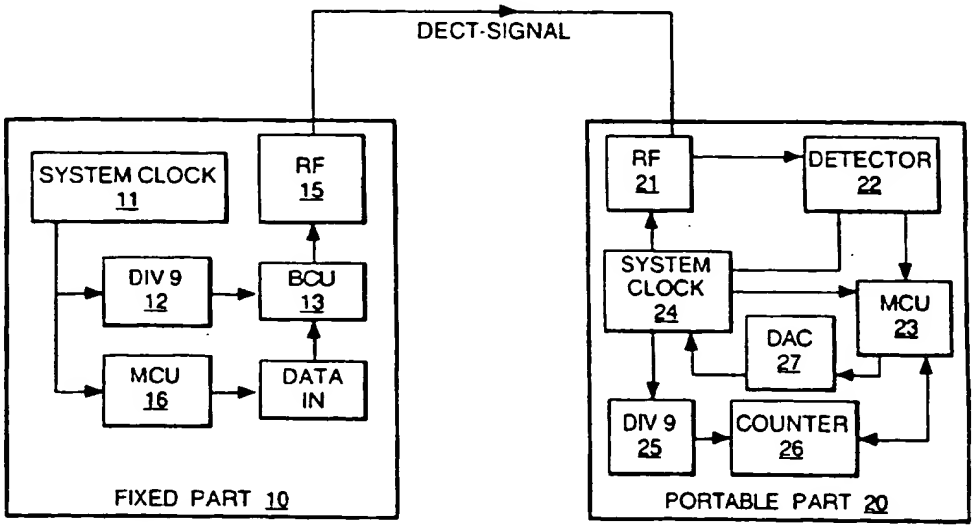
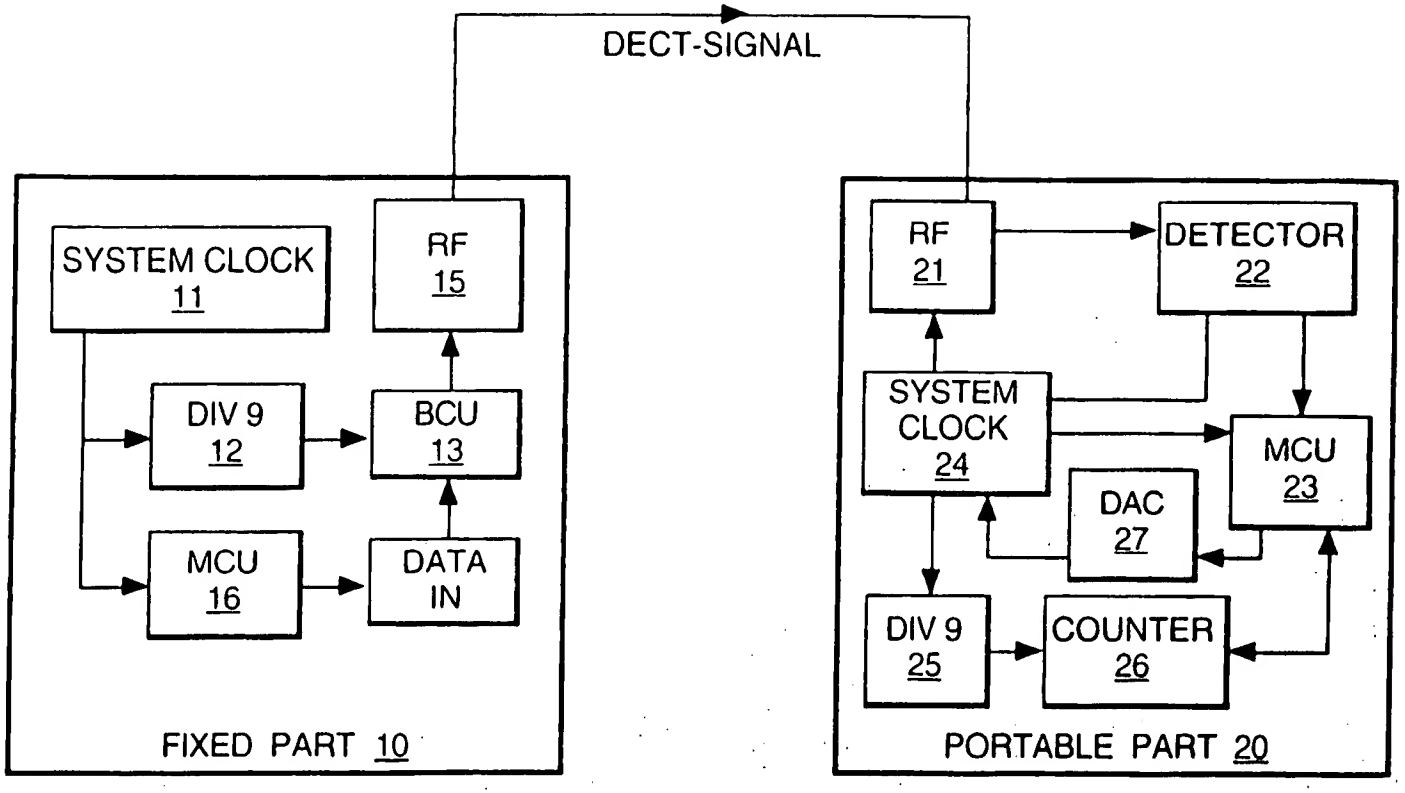
(54) Adjusting radio telephone system clock

(57) A system clock 24 of a radio telephone 20 is adjusted in relation to an associated transmitter/receiver station 10 system clock 11. A predetermined part (SYNC word) which occurs periodically in a digital signal is detected 22. A clock signal having pulses synchronous with the system clock signal of the radio telephone is formed. The clock pulses in the clock signal are counted 26 between the detection of two predetermined parts in the digital signal, and the system clock 24 is corrected in response to the number of pulses between the detection of said two predetermined parts in the digital signal.



GB 2 315 197 A


DECT-SIGNAL
SYSTEM CLOCK
11
RF
15
DIV 9
12
BCU
13
MCU
16
DATA
IN
FIXED PART 10
RF
21
DETECTOR
22
SYSTEM
CLOCK
24
MCU
23
DAC
27
DIV 9
25
COUNTER
26
PORTABLE PART 20

2315197

Method and Apparatus for System Clock Adjustment.

The invention concerns a method of adjusting a radio telephone system clock in relation to an associated transmitter/receiver station system clock, a frequency adjustment device to adjust the radio telephone system clock, and a radio telephone having such a frequency adjustment device.

According to the standard determined by ETSI for the European digital cordless telephone system (DECT), a portable telephone in locked idle mode is to resynchronize its timing in relation to its fixed part with at least a predetermined frequency.

A DECT signal is divided into time slots and frames, where a multiframe consists of 16 frames, and each frame consists of 24 slots (TDMA), each having 480 bits. Since the fixed part transmits data at a bit rate of 1.152 Mbits/sec., 184320 data bits will be transmitted during a multiframe. Even the best system clock (XO) will have an inaccuracy corresponding to at least 6-7 bits during such a period.

One object of the invention is to provide a frequency adjustment device which permits the system clock of the portable part to be adjusted as needed in relation to the system clock of the fixed part.

This object may be achieved by the method of the invention by detecting a predetermined part which occurs periodically in a digital signal. A clock signal synchronous with the radio telephone system clock signal is generated, and the pulses in this clock signal are counted between the detecting times of two predetermined parts in the digital signal. The system clock is corrected in response to the number of pulses between the detection of said two prede-

termined parts of the digital signal. An error signal may be generated, represented by the difference between the number of pulses in the clock signal and the expected number.

In the preferred embodiment, the clock frequency of the clock signal will be selected so as to correspond with the data rate, as the expected number of pulses will hereby correspond to the number of bits in the signal between e.g. two SYNC words. When the voltage dependence of the frequency from the voltage-controlled crystal oscillator is known, a correction voltage may be determined directly on the basis of the pulse difference determined by comparing the counted value with the expected value, thereby enabling correction of the system clock of the portable part to the system clock of the fixed part. This provides a type of phase-locked loop, the system clock of the portable part being corrected at discrete moments. The corrections may be made periodically, or the frequency may be determined by the size of the corrections, said frequency being then increased at greater corrections.

The frequency adjustment device of the invention may adjust the frequency of the radio telephone system clock in relation to an associated transmitter/receiver station system clock and comprise means to detect a predetermined part which occurs periodically in a digital signal, a clock device to supply a clock signal synchronous with the system clock signal, a counter adapted to count the clock pulses in the clock signal of the clock device, and a control device to register the status of the counter device when the detecting means detect the predetermined part in the bit sequence, said control device being moreover adapted to correct the system clock in response to the status of the counter in the detection of the predetermined part. Thus, a form of feedback frequency adjustment is introduced in the system.

When the resynchronization device of the invention is used in a DECT telephone, the detecting means may comprise a SYNC word detector, e.g. a correlator, which correlates the digital signal with a predetermined correlation

word. However, this will be preceded by a search for a preamble, which is a sequence of alternating bits. The SYNC word, which is a predetermined bit pattern determined by ETSI, follows directly after the preamble.

In a preferred embodiment of the invention, the clock device in the frequency adjustment device comprises a first clock (data clock) which supplies a clock signal at 1152 kHz. The system clock of the telephone supplies a clock signal at 10.368 MHz, and the data clock can therefore be provided on the basis of the system clock by dividing its frequency by 9.

In a preferred embodiment, the clock pulses are counted over a multiframe, which corresponds to 184320 data bits, for which reason the counter wraps around at this value. The counter is reset at the value 32 when detecting the SYNC word in the DECT signal, as the SYNC words ends at bit No. 32 in a time slot.

The invention will be explained more fully below, by way of example only, in connection with a preferred embodiment and with reference to the drawing, whose figure schematically shows this embodiment of a frequency adjustment device of the invention for a DECT telephone.

In the preferred embodiment of the frequency adjustment device of the invention, it is used in connection with a DECT system having a signal structure as described in the ETSI proposal for standard ETS 300 175. Data are transferred as time-multiplexed data (TDMA) in time slots according to the DECT standard, and a time slot consists of a preamble having sixteen alternating bits, a SYNC word having sixteen bits in a predetermined bit pattern, data bits and a plurality of terminating control bits. A time slot contains 480 bits in all. Twenty-four successive time slots form a frame, and a telephone connection typically has allocated to it two time slots (one for each way) in the frame. Sixteen frames form a multiframe which has a length of 160 ms because of the signalling rate of 1.152 Mbits/s.

A preferred embodiment of a portable DECT telephone of the invention will be explained in connection with the figure. A fixed part 10 comprises a system clock 11 which oscillates at a frequency of 10.368 MHz. This frequency is divided by a factor 9 in a frequency divider 12, and it is then used in a burst controller unit 13 under the control of a central control unit 16 for transmitting data at a bit rate of 1.152 MHz via an RF part 15.

A portable part 20 (the telephone) receives a time-multiplexed DECT signal via an RF circuit 21. The digital signal is passed from the FM detector of the FR circuit 21 to a detecting device 22, which detects the DECT signal preamble and SYNC word consisting of sixteen alternating bits and sixteen bits in a predetermined bit pattern, respectively. This detection may advantageously be performed with two correlations, where the signal in one of them (the clock recovery unit) is compared with a correlation word corresponding to a section of the preamble and in the other with a correlation word corresponding to the SYNC word.

The clock recovery unit itself is discussed in detail in UK Patent Application No. 9602585.3, and a particularly expedient correlation register is discussed in detail in UK Patent Application No. 9602566.3. These two patent applications are hereby incorporated by reference in the present application. When the preamble has been detected, the SYNC word detecting part of the detector 22 begins to search for the SYNC word, and when the correlation degree exceeds a predetermined threshold value, the SYNC word is considered to be detected, This is described in a co-pending application entitled "Method and Apparatus for Resynchronizing Two System Clocks" (UK No. ...), which concerns synchronization of the portable part and the fixed part in idle mode, and which was filed on the same day as the present application. This patent application is hereby incorporated by reference in the present application.

A full multiframe is run in the preferred embodiment when the system clock, which is also used as a reference frequency in the frequency synthesis via a phase-lock loop (PLL) needs to be adjusted. A counter 26 counts the clock pulses in a clock signal with a frequency of 1152 kHz. This clock signal is supplied from a frequency divider 25 which divides the system clock signal from the system clock 24 of 10.368 MHz by a factor 9. The leading edge of the pulses in the 1152 kHz clock signal will be synchronous with the leading edges on every ninth pulse in the system clock signal. The signals may hereby be considered to be synchronous, even though the frequencies are really a factor 9 different. The portable part clock generator (and thereby the system clock), which supplies a data signal at the data bit rate, must be switched on during the frequency adjustment. This means that the telephone, although it is in idle mode, cannot utilise a sleep mode function, where the system clock is switched off, during the frequency adjustment.

As the SYNC word is terminated 32 bits after the start of the preamble, which starts a time slot, the counter 26 is set at the value 32 when the SYNC word is detected by the detector 23. The counter 26 then counts upwards, and it wraps around at the value 184320 (corresponding to one multiframe). If the system clocks of the fixed part and the portable part are synchronous, a SYNC word will be detected when the counter 26 reaches the value 32. This will not always be the case, as frequency drift may occur. Therefore, the counter 26 is reset at the value 32 when the SYNC word is detected, and the counter value, directly before resetting, is read and used for calculating the difference between the expected value and the actual value in the microcontroller unit 23. This difference is used as a correction value, and by table look-up the MCU 23 can determine a compensation voltage and tune the system clock 24, which is preferably a voltage-controlled temperature-compensated crystal oscillator, via a digital-to-analog converter 27 (DAC).

The system clock of the portable part will hereby be locked to the system clock of the fixed part. The frequency offset value may hereby be kept within a

narrow range, thereby eliminating problems caused by ageing and frequency drift.

The MCU 23 may advantageously have a look-up table in which it can determine the next frequency adjustment time on the basis of the difference. The time for the next frequency adjustment may hereby be postponed if the error is small, or be advanced if the error is great.

CLAIMS

1. A method of adjusting a radio telephone system clock in relation to an associated transmitter/receiver station system clock, comprising detecting a predetermined part which occurs periodically in a digital signal, providing a clock signal which is synchronous with the system clock signal of the radio telephone, counting the clock pulses in the clock signal between the detection of two predetermined parts in the digital signal, and correcting the system clock in response to the number of pulses between the detection of said two predetermined parts in the digital signal.

2. A method according to claim 1, wherein the digital signal is a DECT signal, and wherein the two predetermined parts comprise the signal preamble and SYNC word occurring in two different time slots.

3. A method according to claim 1 or 2, wherein a correction voltage is generated to correct the system clock in response to the number of pulses in relation to a predetermined value.

4. A frequency adjustment device for a radio telephone to adjust the frequency of a radio telephone system clock in relation to an associated transmitter/receiver station system clock, comprising means to detect a predetermined part which occurs periodically in a digital signal, a clock device to supply a clock signal which is synchronous with the system clock signal, a counter device adapted to count the clock pulses in the clock signal of the clock device, and a control device to register the status of the counter device when the detecting means detect the predetermined part in the digital signal, said control device being moreover adapted to correct the system clock in response to the status of the counter device in the detection of the predetermined part.

5. A frequency adjustment device according to claim 4, wherein the detecting means comprise a SYNC word detector to detect the SYNC word in a DECT signal.

6. A frequency adjustment device according to claim 4 or 5, wherein the clock device supplies the clock signal by dividing the system clock frequency by means of a frequency divider.

7. A frequency adjustment device according to claim 6, wherein the clock device supplies the clock signal with a frequency of 1152 kHz by dividing the system clock with a frequency of 10.368 MHz by means of a frequency divider which divides the system clock frequency by a factor 9.

8. A frequency adjustment device according to any of claims 4-7, wherein the digital signal is a DECT signal, and wherein the counter device counts the pulses in the clock signal over a plurality of frames in the DECT signal.

9. A frequency adjustment device according to claim 8, wherein the counter device counts the pulses in clock signals over a multiframe.

10. A frequency adjustment device according to claims any of 4-9, wherein the control device, when the detecting means detect the predetermined part in the form of a SYNC word, generate an error signal in response t the status of the counter device, said error signal being used for correcting the system clock.

11. A frequency adjustment device according to claim 10, wherein the control device is associated with a digital-to-analog converter to which the error signal is fed, said converter generating an analog control voltage contribution which is fed to the system clock.

12. A frequency adjustment device substantially as described in the foregoing with reference to the figure of the accompanying drawing.

13. A radio telephone having a frequency adjustment device according to any of claims 4-12.

The Patent Office

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Application No: GB 9614537.0
Claims searched: 1-13

Examiner: Simon Rees
Date of search: 4 October 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4M (MTA1-3, MTSX1-3), H4P (PPF, PSB, PSEX), H4L (LDLX, LDSX)

Int Cl (Ed.6): H04J (3/06), H04L (7/08, 7/10), H04Q (7/30

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP0338668A2	(GEC) Whole document, especially lines 7-27 of column 3.	1, 3, 4, 11.
A, &	US5070517A	(Köchler) Whole document, especially summary and from line 43 of column 4 to line 5 of column 5.	1, 3, 4, 11.
A	US4144414A	(Nicholas) Whole document.	1, 4.
A, &	EP0318689A2 is noted as being an equivalent document to US5070517A above.		1, 3, 4, 11.

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.